A Bidirectional Non-Isolated Multi-Input DC-DC Converter for Hybrid Energy Storage Systems in Electric Vehicles

F. Akar, Y. Tavlasoglu, E. Ugur, B. Vural, I. Aksoy

***Abstract*—In order to process the power in hybrid energy systems using reduced part count, reseachers have proposed several multi-input dc-dc power converter topologies to transfer power from different input voltage sources to the output. This paper proposes a novel bidirectional non-isolated multi-input converter (MIC) topology for hybrid systems to be used in electric vehicles composed of energy storage systems (ESSs) with different electrical characteristics. The proposed converter has the ability of controlling the power of ESSs by allowing active power sharing. The voltage levels of utilized ESSs can be higher or lower than the output voltage. The inductors of the converter are connected to a single switch; therefore, the converter requires only one extra active switch for each input unlike its counterparts, hence results in reduce element count. The proposed MIC topology is compared with its counterparts concerning various parameters. It is analyzed in detail, then this analysis is validated by simulation and a 1 kW protoype based on a battery/ultra-capacitor (UC) hybrid ESS.**

***Index Terms*— Batteries, bidirectional, hybrid energy storage systems, ultra-capacitors, multi-input converter**

I. INTRODUCTION

There is a lot of research conducted on hybrid electric vehicles (HEVs), electric vehicles (EVs), and plug-in hybrid electric vehicles (PHEVs) due to the environmental and economic concerns [1]–[3] in which hybrid energy storage systems (HESSs) have been comprehensively studied. The aim of a HESS is to make use of strong features of ESS elements while eliminating their weaknesses to reach the performance of an ideal ESS element [3]. In order to create a HESS having the characteristics of an ideal energy storage unit such as high energy/power density, low cost/weight per unit capacity, and long cycle life, researchers have hybridized batteries and ultracapacitors (UCs) in [4]–[7]. The active hybridization of the aforementioned ESSs, in which the power/current of the ESS can be controlled fully, is only possible by means of utilizing power converters.

Power converter topologies used in HESS can be classified into two main categories, i.e., isolated and non-isolated. In [8]–[11], isolated HEES system topologies include a transformer to offer galvanic isolation between sources and output. Non-isolated power converters are much simpler in terms of design and control when compared to isolated ones. One of the simplest way to build a non-isolated HESS is to connect some of the sources directly while linking others to dc bus via bidirectional dc-dc converters as in [12], [13]; however, this method does not allow to adjust the dc bus voltage. In addition, studies in [14]–[18] propose individual dc-dc converters for each input. Unlike the former topology, the multiple converter topology structure enables managing the output voltage; however, it is an expensive approach as it requires multiple converters. In order to decrease the cost of multiple converter topologies, multi input converter (MIC) topologies are reported in the literature [19]–[22]. As mentioned in [19], MICs are not only cost-effective; but also reliable, simple, and easy to control. In [20], a bidirectional MIC having a single inductor shared by input sources is proposed; although this converter has the advantage of being simple, unfortunately, it does not allow active power sharing between sources. In [21], authors offer a multi input dc-dc/ac boost converter which contains a bidirectional port for battery storage in addition to several unidirectional ports for dc sources; therefore, it can be asserted that this converter does not offer flexibility in terms of the number of EES elements. In [22], authors suggest a bidirectional MIC called multiple-input power electronics converter (MIPEC) whose input ports connected to dc bus via half bridges as shown in Fig.1(a); it can successfully control charge/discharge currents of input sources whose voltages are required to be less than the output voltage.

In [23], a modified boost converter is introduced; this converter is constructed in a way that the classical boost converter inductor is replaced with a coupled inductor and a high valued capacitor; here, the input current ripple is aimed to be eliminated via a single switch driving the input source energy and energy stored in the capacitor. Based on this concept, a non-isolated unidirectional double input dc-dc power converter is proposed in [24]. In this paper, instead of the high valued capacitor in [23], the author utilized an EES element, namely a UC, which is essentially a capacitor with large capacitance. The motivation of [24] is to create an

Manuscript received July 3, 2015; revised October 5,2015, accepted October 27, 2015. This work was supported in part by The Scientific and Technological Reseach Council of Turkey (TUBITAK) under Grant 113M088.

Authors are with Electrical Engineering Department, Yildiz Technical University,Esenler, Istanbul, 34220, Turkey. (e-mail: fakar@yildiz.edu.tr, y.tavlasoglu06@gmail.com, enesugur@yildiz.edu.tr, bvural@yildiz.edu.tr, iaksoy@yildiz.edu.tr)

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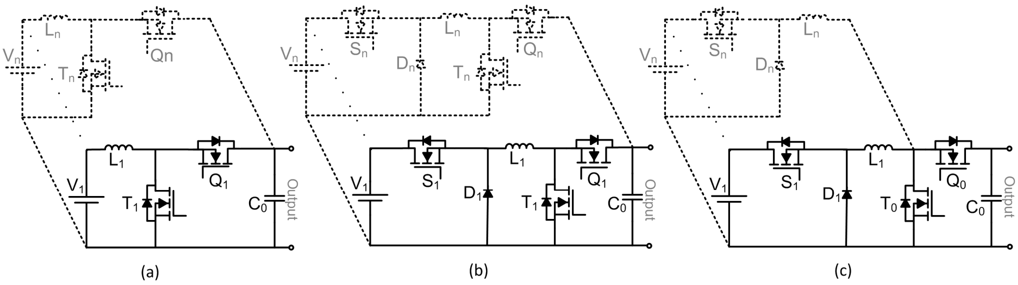

(a) (b) (c)

Fig. 1. Bidirectional multi input dc/dc converters. a) Mutiple-input power electronics converter (MIPEC). b) Modified cascaded buck-boost converter (CBBC) approach. c) Proposed converter

FC/UC hybrid system to smooth FC current thanks to UC. As distinct from the converter in [23], the proposed converter in [24] includes one pair of a switch and a diode added to both inputs hence makes possible active power sharing between sources as well as control of dc bus voltage level; this converter is then modified by replacing its output diode with a switch in [25] for battery/UC hybridization for an EV application. This modification transforms the converter into a bidirectional converter that can store regenerative braking energy in battery and UC according to their characteristics. The paper presented in [25] is the source of motivation of this work. The proposed bidirectional non-isolated dc-dc converter topology in this work and its counterparts are shown in Fig. 1. In summary, they all require separate inductors for each input and allow active power sharing between their input sources. This paper compares the proposed converter with its counterparts and gives a detailed analysis along with its verification based on the simulation and experiment results. The system is examined on a battery/UC HESS, which is a widely used configuration as it can satisfy the requirements for an EV such as high power/energy density and improved battery life span [13], [26], [27]. This paper is organized as follows. Section II compares the proposed converter with its candidate counterparts. Section III gives the analysis of converter operating modes. In Section IV, small signal modeling of the converter and controller details are given. Section V validates the analysis by illustrating the simulation and experimental results.

II. A Comparative Analysis

In Table I, three topologies given in Fig. 1 are compared concerning various parameters. As can be seen from this table, MIPEC illustrated in Fig. 1(a) provides boost and buck operations during propulsion and regenerative braking, respectively. The topology given in Fig 1(b) basically consists of modified version of separate cascaded buck-boost converters (CBBC) [28] branches that are connected in parallel; when compared to MIPEC, this topology enables buck operation as well during propulsion. Note that the modified CBBC is considered here for the sake of fair comparison in terms of active switch count. The proposed converter in this paper which is given in Fig. 1(c) has also buck/boost capability during propulsion with the advantage of fewer active switch requirement as stated in Table I. Table I also includes the switch stress analysis of examined converters. Here it is assumed that each input source equally shares the output power in both directions. Since T_0 and Q_0 in the proposed converter handle all the power, it seems that these two switches suffer from high current stress thus need to be bulkier than other switches in an application. However, for a robust HESS with a multi-input converter, every branch of that converter needs to be designed considering the possibility that the associated input source solely undertakes or stores all

TABLE I
Comparison of Bidirectional Multi-Input Converters

			MIPEC	Modified CBBC approach	Proposed
Operation mode during propulsion/reg. braking			Boost/ buck	Buck*- boost**/ buck	Buck-boost/ buck
Number of active switches (n is number of inputs)			$2\times n$	$3\times n$	$2+n$
Switch stresses during propulsion/ reg. braking ($i = 1, 2 \ldots n$)	S_i	Vol.	-	V_i	V_i
		Cur.	-	$\alpha\frac{V_i}{V_o}p.u./$ $\frac{V_o}{V_i}p.u.$	$\frac{1}{d_{Si}}p.u./$ $\frac{V_o}{V_i}p.u.$
	T_o and T_i	Vol.	V_o	V_o	V_o
		Cur.	$1p.u./$ $\frac{V_o}{V_i}p.u.$	$\beta p.u./$ $\frac{V_o}{V_i}p.u.$	$\frac{n}{d_{Si}}p.u./$ $\frac{nV_o}{V_i}p.u.$
	Q_0 and Q_i	Vol.	V_o	V_o	V_o
		Cur.	$1p.u./$ $\frac{V_o}{V_i}p.u.$	$\alpha\frac{V_i}{V_o}p.u./$ $\frac{V_o}{V_i}p.u.$	$\frac{n}{d_{Si}}p.u./$ $\frac{nV_o}{V_i}p.u.$
Overall eff.	1^{st} case: V_1=36V, V_2=36V, V_o=48V.	During prop.	96.02%	95.97%	95.81%@ d_{T0}=0.25 94.07%@d_{T0}=0.5 87.59%@d_{T0}=0.75
		During reg. braking	95.88%	94.12%	94.27%
		Average	96%	95.71%	95.59%@d_{T0}=0.25 94.09%@d_{T0}=0.5 88.55%@d_{T0}=0.75
	2^{nd} case: V_1=60V, V_2=36V, V_o=48V.	During prop.	N/A	95.98%	95.46%@ d_{T0}=0.25 93.71%@d_{T0}=0.5 87.23%@d_{T0}=0.75
		During reg. braking		%95.39	95.39%
		Average		%95.89	95.45%@d_{T0}=0.25 93.97%@d_{T0}=0.5 88.39%@d_{T0}=0.75
* $\alpha=1$, β=0. ** $\alpha=V_o/V_i$, β=1.					

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of the output power; therefore, it can be declared that all switches in the proposed converter should have same or similar current ratings.

In Table I, efficiency comparison of the examined converters is given. In this work, the switching frequency is 20 kHz and the converters have two input sources. The procedure given in [4] is followed to calculate switching, conduction and inductor losses. Then overall efficiencies under the load variations depending on ECE-15 driving cycle for two different cases are determined. For a realistic calculation, the parameters of commercial elements, namely, FDP036N10A as power switch, MBR4060PT as power diode, 150 µH inductors having 00K8020E026 magnetic cores and 40 mΩ serial resistances, are considered. As can be seen from the results, in the first case, MIPEC is the most efficient converter due to less number of switches. During the propulsion, the proposed converter exhibits the lowest efficiency, particularly because of increasing switching and conduction losses. It is interesting that its efficiency changes depending on the duty cycle of T_0 since it affects the current stress. Additionally, during the regenerative braking, the proposed converter is more efficient than the modified CBBC approach since it utilizes fewer active switches thus decreases switching losses. In the second case, the voltage of one input is raised to 60 V to evaluate the buck operation. In this setup, it is clear that MIPEC is not operational. Moreover, other two converters can store the regenerative braking energy into only one input source. During the propulsion, the efficiency of proposed converter decreases in comparison to the first case due to the increasing current stresses. In a similar way, the efficiency of proposed converter in the second case depends on d_{T0}. Here the proposed topology is again slightly worse than the other topology in terms of efficiency. During the regenerative braking, both converters have the same efficiency since they have same equivalent circuit in the second setup. Overall, the proposed converter exhibits slightly worse efficiency than others in both cases on account of a reduction in active switch count. Note that in the efficiency analyze above, MIPEC, modified CBBC approach, and the proposed converter have 4, 6 and 4 active switches, respectively.

III. THE ANALYSIS OF THE PROPOSED CONVERTER

The proposed multi-input bidirectional dc-dc converter is analyzed in the case that it has two inputs as illustrated in Fig. 2. As can be seen, the converter has four power switches with internal diodes, two power diodes and two inductors. S_1, S_2, T_0, and Q_0 are pulse width modulation (PWM) controlled switches with d_{S1}, d_{S2}, d_{T0}, and d_{Q0} duty cycles, respectively.

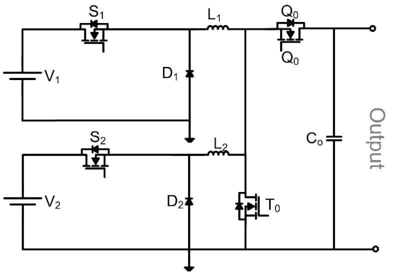

Fig. 2. Proposed multi-input converter with two inputs

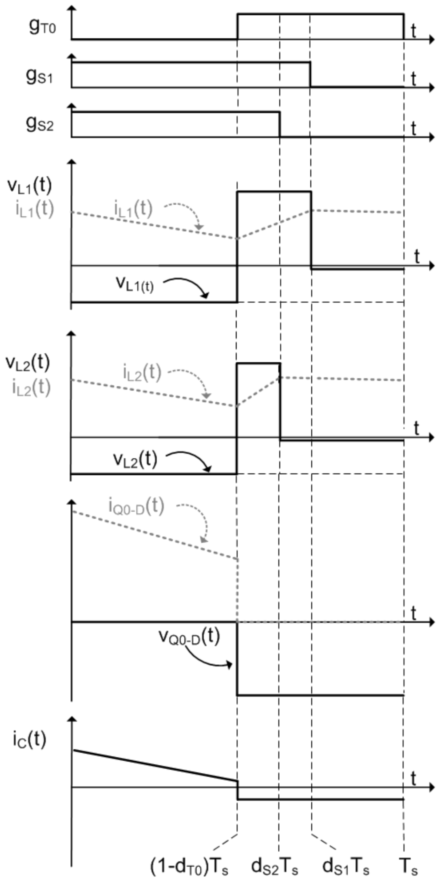

Fig. 3. Typical waveforms in the discharging mode

The proposed converter has mainly two different operation modes. The first operation mode is called discharging mode. In this mode, the output is fed by input sources according to states of S_1, S_2 and T_0. Power diodes D_1 and D_2 operate in complementary manner with S_1 and S_2, respectively. The second operation mode is called charging mode. In the charging mode, by controlling Q_0, regenerative braking energy charges ESSs depending on their voltage levels. Note that, if there is need for an option whether or not to charge one of the ESSs, a solid-state switch (e.g. a reverse connected MOSFET) can be added to the associated converter input. In the charging mode, D_1 and D_2 are always OFF while the body diode of T_0 carries the inductor currents when Q_0 is OFF. In analysis, it is assumed that inductors, body diodes of switches, and power diodes are ideal while the switch turn-ON resistances (R_{dson}) and output capacitor equivalent serial resistance (R_C) are taken into account; in addition, the converter operates in continuous conduction mode (CCM).

A. *Discharging Mode*

In the discharging mode, one switching cycle consists of four subintervals. Typical waveforms in the discharging mode are illustrated in Fig. 3. In this figure, it is obvious that $d_{T0}<d_{S2}<d_{S1}$ according to the assumption that $V_1< V_2<V_o$, where V_1 is the first input voltage, V_2 is the second input

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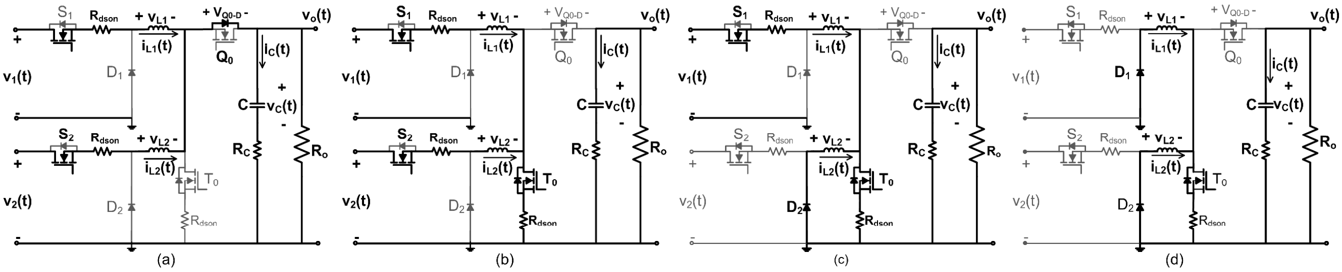

Fig. 4. Equivalent circuits in the discharging mode. (a) Switching subinterval 1: $0<t<(1-d_{T0})T_s$. (b) Switching subinterval 2: $(1-d_{T0})T_s<t<d_{S2}T_s$. (c) Switching subinterval 3: $d_{S2}T_s<t<d_{S1}T_s$. (d) Switching subinterval 4: $d_{S1}T_s<t<T_s$.

voltage, and V_o is the output voltage. The relationship between the voltage levels and duty cycles will be explained in detail later on. Steady state equivalent circuits in four subintervals are demonstrated in Fig. 4.

Switching subinterval 1 $[0<t<(1-d_{T0})T_s]$: S_1 and S_2 are turned ON while S_0 is turned OFF. D_1 and D_2 are OFF as shown in Fig. 4(a). Due to the negative voltages across inductors, their currents decrease. In addition, the current through the body diode of Q_0 is equal to the sum of inductor currents, and it charges the output capacitor.

Switching subinterval 2 $[(1-d_{T0})T_s<t<d_{S2}T_s]$: According to Fig. 4(b), at $t=(1-d_{T0})T_s$, T_0 is turned ON while S_1 and S_2 are still conducting, and diodes D_1 and D_2 are still OFF. In this subinterval, inductors start to be charged due to positive voltage while the output capacitor discharges to feed the load.

Switching subinterval 3 $[d_{S2}T_s<t<d_{S1}T_s]$: At $t=d_{S2}T_s$, S_2 is turned OFF whereas S_1 and T_0 are still ON. In this subinterval, D_2 starts to conduct as shown in Fig. 4(c). As can be seen, L_1 current starts to decrease slowly due to the turn-on resistance of T_0. Besides, L_1 continues to be charged, D_1 is still OFF, and output capacitor still discharges.

Switching subinterval 4 $[d_{S1}T_s<t<T_s]$: Last switching subinterval is initiated by turning OFF S_1 at $t=d_{S1}T_s$ as demonstrated in Fig. 4(d). Both D_1 and D_2 become conducting and both inductor currents are decreasing because of the turn-on resistance of S_0. Moreover, the output capacitor current is still negative.

Finally, equations that show voltage variations of L_1 and L_2 in the discharging mode can be written as given in (1) and (2), respectively.

$$v_{L1}(t)=\begin{cases} v_1(t)-v_o(t)-R_{dson}i_{L1}(t), & 0<t<(1-d_{T0})T_s \\ v_1(t)-R_{dson}\left(2i_{L1}(t)+i_{L2}(t)\right), & (1-d_{T0})T_s<t<d_{S1}T_s \\ -R_{dson}\left(i_{L1}(t)+i_{L2}(t)\right), & d_{S1}T_s<t<T_s \end{cases} \tag{1}$$

$$v_{L2}(t)=\begin{cases} v_2(t)-v_o(t)-R_{dson}i_{L2}(t), & 0<t<(1-d_{T0})T_s \\ v_2(t)-R_{dson}\left(i_{L1}(t)+2i_{L2}(t)\right), & (1-d_{T0})T_s<t<d_{S2}T_s \\ -R_{dson}\left(i_{L1}(t)+i_{L2}(t)\right), & d_{S2}T_s<t<T_s \end{cases} \tag{2}$$

The output capacitor current and output voltage variations depending on the state of the S_0 can be derived as given in (3) and (4).

$$i_C(t)=\begin{cases} \dfrac{R_o\left(i_{L1}(t)+i_{L2}(t)\right)}{R_o+R_c}-\dfrac{1}{R_o+R_c}v_C(t), & 0<t<(1-d_{T0})T_s \\ -\dfrac{1}{R_o+R_c}v_C(t), & (1-d_{T0})T_s<t<T_s \end{cases} \tag{3}$$

$$v_o(t)=\begin{cases} \dfrac{R_oR_c}{R_o+R_c}\left(i_{L1}(t)+i_{L2}(t)\right)+\dfrac{R_o}{R_o+R_c}v_C(t), & 0<t<(1-d_{T0})T_s \\ \dfrac{R_o}{R_o+R_c}v_C(t), & (1-d_{T0})T_s<t<T_s \end{cases} \tag{4}$$

Based on small ripple approximation and inductor volt-second-balance [29], by utilizing (1) and (2), the relationship between the output voltage and source voltages at steady state can be obtained as given in (5) by neglecting R_{dson}.

$$V_o=V_1\frac{d_{S1}}{1-d_{T0}}=V_2\frac{d_{S2}}{1-d_{T0}} \tag{5}$$

According to (5), the converter operates at an equilibrium point where duty cycles have following relationship:

$$\frac{V_1}{V_2}=\frac{d_{S2}}{d_{S1}} \tag{6}$$

B. Charging Mode

In the charging mode, Q_0 is controlled and T_0 is kept OFF in order to store regenerative braking energy into the energy storage units while regulating the output voltage. As expressed, charging only one ESS can be realized by adding a solid-state switch to the converter input. Therefore, in this

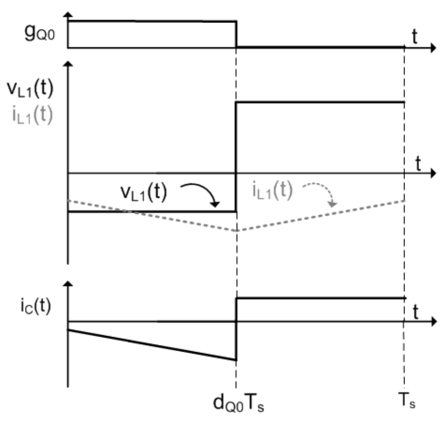

Fig. 5. Typical waveforms in the charging mode

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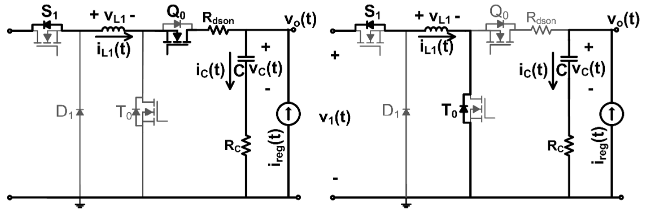


(a) (b)

Fig. 6. Equivalent circuits in charging mode. (a) Switching subinterval 1: $0<t<d_{Q0}T_s$. (b) Switching subinterval 2: $d_{Q0}T_s<t<T_s$.

analysis, it is assumed that the regenerative braking energy charges only the first input. Furthermore, since the proposed converter operates in buck mode in the charging mode, the output voltage is assumed to be higher than V_1.

Fig. 5 illustrates the steady state waveforms in the charging mode. According to this figure, one switching cycle is composed of two subintervals. Associated equivalent circuits are shown in Fig.6 where $i_{reg}(t)$ is the current source that represents the regenerative braking energy. In this mode, the inductor current is negative since the source is charged.

Switching subinterval 1 [$0<t<d_{Q0}T_s$]: From Fig. 6(a) one can see that, when Q_0 is turned ON, the body diode of S_0 becomes OFF. Because of negative voltage across L_1, its current increases (negatively). Moreover, the current of the output capacitor is negative since it discharges.

Switching subinterval 2 [$d_{Q0}T_s<t<T_s$]: At $t=d_{Q0}T_s$, Q_0 is turned OFF. Therefore, the current of L_1 now flows through T_0 body diode as illustrated in Fig. 6(b). In this subinterval, the inductor current decreases due to the source voltage across it. Additionally, the current of output capacitor changes its direction and becomes positive.

Based on the analysis above, the equations for the L_1 voltage, output capacitor current, and output voltage in two switching subintervals can be given as given in (7), (8), and (9), respectively.

$$v_{L1}(t)=\begin{cases} v_1(t)-v_o(t)-R_{dson}i_{L1}(t), & 0<t<d_{Q0}T_s \\ v_1(t), & d_{Q0}T_s<t<T_s \end{cases} \tag{7}$$

$$i_C(t)=\begin{cases} i_{L1}(t)+i_{reg}(t), & 0<t<d_{Q0}T_s \\ i_{reg}(t), & d_{Q0}T_s<t<T_s \end{cases} \tag{8}$$

$$v_o(t)=\begin{cases} \left(i_{L1}(t)+i_{reg}(t)\right)R_c+v_C(t), & 0<t<d_{Q0}T_s \\ i_{reg}(t)R_c+v_C(t), & d_{Q0}T_s<t<T_s \end{cases} \tag{9}$$

Applying to small ripple approximation and inductor volt-second-balance to (7), one can find the relationship between the output voltage (V_o) and source voltage (V_1) at steady state as in (10) by neglecting R_{dson}.

$$V_o=\frac{V_1}{d_{Q0}} \tag{10}$$

IV. SMALL SIGNAL MODELING AND CONTROLLER CONSIDERATIONS

A. Small Signal Modeling

In [30], authors propose the unified controller concept. According to this concept, a single controller can be used for buck mode (charging) and boost mode (discharging) of a bidirectional converter; and that controller can be designed according to one of the transfer functions of these two operating modes. Therefore, in this paper, a classical boost converter is analyzed for the charging mode. Similarly, switch turn-ON resistance of this boost converter and the equivalent serial resistance of the output capacitor are taken into account, while inductor resistance and voltage drops on diodes are ignored. Since related equations to this non-ideal boost converter can be derived easily in a similar way of deriving (1)-(4) and (7)-(9), they are not given here.

A small signal ac model in matrix form can be given in (11) where A, B, and C are matrices comprised of constants.

$$A\hat{x}(s)=B\hat{d}(s)+C\hat{v}(s) \tag{11}$$

In (11), $x(s)$, $d(s)$, and $v(s)$ denote the state variables, duty cycles, and input voltages, respectively, which consist of dc components (X, D, and V) and small perturbations ($\hat{x}(s)$, $\hat{d}(s)$, and $\hat{v}(s)$) as shown in (12).

$$x=X+\hat{x}(s); \qquad d=D+\hat{d}(s); \qquad v=V+\hat{v}(s). \tag{12}$$

In order to obtain A, B, and C matrices in (11), first (12) is applied to (1)-(4) and to the derived equations for non-ideal boost converter. By applying Laplace transform to these equations, they are averaged over one switching cycle and second order ac terms are neglected [29]. Finally, the small signal ac models in matrix form of the converter in the discharging mode and charging mode are derived as in (13) and (14), respectively.

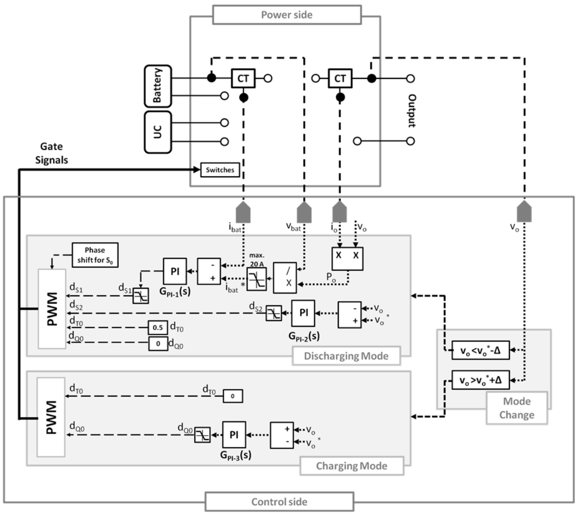


Fig. 7. Overall control strategy

$$A=\begin{bmatrix} sL_1+\left(D_{T0}+D_{S1}\right)R_{dson} & R_{dson} & 0 & -\left(1-D_{T0}\right) \\ R_{dson} & sL_2+\left(D_{T0}+D_{S2}\right)R_{dson} & 0 & -\left(1-D_{T0}\right) \\ \left(1-D_{T0}\right)\dfrac{R_o}{R_o+R_C} & \left(1-D_{T0}\right)\dfrac{R_o}{R_o+R_C} & -\left(sC+\dfrac{1}{R_o+R_C}\right) & 0 \\ \left(1-D_{T0}\right)\dfrac{R_oR_C}{R_o+R_C} & \left(1-D_{T0}\right)\dfrac{R_oR_C}{R_o+R_C} & \dfrac{R_o}{R_o+R_C} & -1 \end{bmatrix},\quad B=\begin{bmatrix} V_o-I_{L1}R_{dson} & V_1-I_{L1}R_{dson} & 0 \\ V_o-I_{L2}R_{dson} & 0 & V_2-I_{L2}R_{dson} \\ \left(I_{L1}+I_{L2}\right)\dfrac{R_o}{R_o+R_C} & 0 & 0 \\ \left(I_{L1}+I_{L2}\right)\dfrac{R_oR_C}{R_o+R_C} & 0 & 0 \end{bmatrix},$$

$$C=\begin{bmatrix} D_{S1} & 0 \\ 0 & D_{S2} \\ 0 & 0 \\ 0 & 0 \end{bmatrix},\quad \hat{x}(s)=\begin{bmatrix} \hat{i}_{L1}(s) \\ \hat{i}_{L2}(s) \\ \hat{v}_c(s) \\ \hat{v}_o(s) \end{bmatrix},\quad \hat{d}(s)=\begin{bmatrix} \hat{d}_{T0}(s) \\ \hat{d}_{S1}(s) \\ \hat{d}_{S2}(s) \end{bmatrix},\quad \hat{v}(s)=\begin{bmatrix} \hat{v}_1(s) \\ \hat{v}_2(s) \end{bmatrix}. \tag{13}$$

$$A=\begin{bmatrix} sL_1+D_{Q0}R_{dson} & 0 & \left(1-D_{Q0}\right) \\ \left(1-D_{Q0}\right)\dfrac{R_o}{R_o+R_C} & -\left(sC+\dfrac{1}{R_o+R_C}\right) & 0 \\ \left(1-D_{Q0}\right)\dfrac{R_oR_C}{R_o+R_C} & \dfrac{R_o}{R_o+R_C} & -1 \end{bmatrix},\quad B=\begin{bmatrix} V_o \\ I_{L1}\dfrac{R_o}{R_o+R_C} \\ I_{L1}\dfrac{R_oR_C}{R_o+R_C} \end{bmatrix},\quad C=\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix},\quad \hat{x}(s)=\begin{bmatrix} \hat{i}_{L2}(s) \\ \hat{v}_c(s) \\ \hat{v}_o(s) \end{bmatrix},\quad \hat{d}(s)=\hat{d}_{Q0}(s);\ \hat{v}(s)=\hat{v}_1(s). \tag{14}$$

B. Control Strategy

A battery/UC HESS is considered here in order to test the proposed converter, and the control strategy which is demonstrated in Fig. 7 is applied to system. In this figure, the power side represents the proposed power converter where CT denotes current transducers. In addition, the control side is the platform where currents and voltages are sensed and developed control strategy is carried out. In the control side, first of all, the operation mode is determined by checking the output voltage (v_o): the discharging mode is activated when v_o is lower than $v_o^*-\Delta$ and the charging mode is activated when v_o is greater than $v_o^*+\Delta$, where v_o^* is the output voltage reference and Δ is a defined voltage level.

In the discharging mode, it is aimed to realize active power sharing between battery and UC. In order to achieve this, a PI controller adjusts the duty cycle of S_1 to control the battery power while another PI controller adjusts the duty cycle of S_2 for dc bus regulation. In this way, UC power is controlled ultimately since battery and UC share the output power demand. The battery current reference is calculated to assure that battery provides all of the power demand by load providing that it does not exceed 20 A. In the case that battery power is not enough to regulate dc bus, UC undertakes the necessary extra power. From (5), one can see that increasing d_{T0} expands the ESS voltage range. However, it may result in reduction in the efficiency as highlighted in the efficiency analysis. Therefore, in the discharging mode, d_{T0} is kept constant at a reasonable value, 0.5, and uncontrolled for the sake of control simplicity. In the charging mode, Q_0 duty cycle is regulated by a PI controller to keep the output voltage at its reference while keeping T_0 always OFF. It is highlighted that the voltage error in the charging mode is calculated by v_o-v_o^* since the inductor current changes its direction.

C. Controller Design

In order to design PI controllers shown in Fig. 7, first of all associated transfer functions need to be known. Transfer function matrices can be obtained by solving small signal model in (11) for each operation mode as given in (15).

$$\hat{x}(s)=A^{-1}B\hat{d}(s)+A^{-1}C\hat{v}(s) \tag{15}$$

If the effect of cross-coupling transfer functions in (15) is assumed to be negligible, decoupled transfer function can be derived as in [22], [31]–[33] . Therefore, by letting other perturbations be zero in (15), control-to-inductor current transfer function and control-to-output transfer function for the discharging mode and control-to-output transfer function for the charging can be found. After this step, control-to-battery current transfer function can be derived as given in (16).

$$\frac{\hat{i}_{bat}(s)}{\hat{d}_{S1}(s)}=\frac{\hat{i}_{L1}(s)}{\hat{d}_{S1}(s)}D_1+I_{L1} \tag{16}$$

The generalized form of a second-order transfer function can be shown as in (17). Using (15), the coefficients in (17) for both operation modes can be calculated as given in Table II and Table III.

$$G(s)=\frac{b_0+b_1s+b_2s^2}{a_0+a_1s+a_2s^2} \tag{17}$$

PI controllers are used to improve phase margins and to have reasonable cut-off frequencies. A PI controller transfer function is given (18).

$$G_{PI}(s)=K_p+\frac{K_i}{s} \tag{18}$$

In this work, PI controller gains are determined as shown in Table IV by using PID Tuning tool in Matlab®. Fig. 8 and Fig. 9 demonstrate the uncompensated and compensated system bode plots for the discharging and charging modes, respectively. From these figures it can be seen that, all of the compensated systems have positive phase margins hence they are stable [29]. Moreover, decreased cut-off frequencies result in low gain in high frequencies; therefore, increase the robustness [17]. Note that parameters given in Table V are utilized to derive bode plots and design the controllers.

V. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the analysis and evaluate the dynamic performance of the converter, a 1 kW prototype is built as illustrated in Fig. 10. As can be seen from this figure, the converter consists of a power board and a control board. The power board includes the power elements such as, switches, gate drivers, diodes, with specifications given in Table VI.

In Table VI, d_{T0} is limited between 0.4 and 0.6 to assure that the converter can work in both directions according to the input and output voltage ranges determined concerning the rating of power elements. The control board includes Texas Instrument TMS320F28335 DSP as a controller and an interface to program it directly via a USB port of a computer.

TABLE II
DISCHARGING MODE TRANSFER FUNCTION COEFFICIENTS

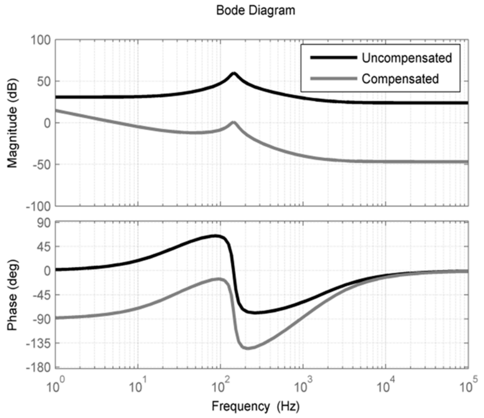
	$\hat{i}_{bat}(s)/\hat{d}_{S1}(s)$	$\hat{v}_o(s)/\hat{d}_{S2}(s)$
a_0	$D_{T0}^{'}{}^2R_o+\left(D_{T0}+D_{S1}\right)R_{dson}$	
a_1	$L_{1,2}+(R_o+R_C)\left(D_{T0}+D_{S1}\right)\left(R_{dson}+D_{T0}^{'}{}^2R_oR_C\right)C$	
a_2	$(R_C+R_o)L_{1,2}C$	
b_0	$D_{S1}(V_{bat}-I_{L1}R_{dson})+I_{L1}a_0$	$D_{T0}^{'}\left(V_{UC}-I_{L2}R_{dson}\right)\times \left(\frac{R_o^2}{R_o+R_C}+\frac{R_C}{R_o+R_C}\right)$
b_1	$D_{S1}(V_{bat}-I_{L1}R_{dson})\left(R_C+R_o\right)C+$ $I_{L1}a_1$	$D_{T0}^{'}\left(V_{UC}-I_{L2}R_{dson}\right)\left(R_oR_CC\right)$
b_2	$I_{L1}a_2$	0

TABLE III
CHARGING MODE TRANSFER FUNCTION COEFFICIENTS

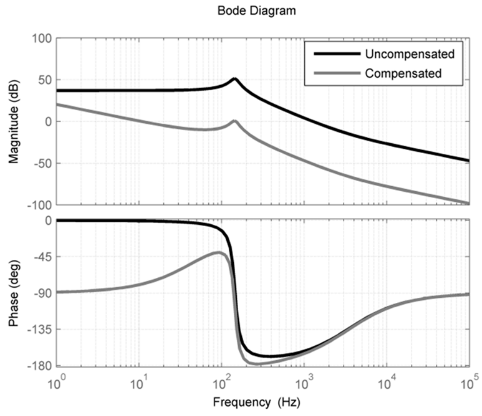
	$\hat{v}_o(s)/\hat{d}_{Q0}(s)$
a_0	$D_{Q0}^{'}{}^2R_o+D_{Q0}R_{dson}$
a_1	$L_2+\left(R_C+R_o\right)D_{Q0}\left(R_{dson}+D_{Q0}C\right)$
a_2	$(R_C+R_o)L_2C$
b_0	$V_oD_{Q0}^{'}R_o-I_{L2}R_oR_{dson}D_{Q0}$
b_1	$V_oD_{Q0}^{'}R_oR_CC-I_{L2}R_o\left(L_2+D_{Q0}R_{dson}R_CC\right)$
b_2	$-I_{L2}R_oR_CL_2C_0$

TABLE IV
CONTROLLER PARAMETERS

	Discharging mode		Charging mode
	$G_{PI-1}(s)$	$G_{PI-2}(s)$	$G_{PI-3}(s)$
K_p	0.000291	0.00278	0.011414
K_i	0.98979	0.92074	0.37555



(a)



(b)

Fig. 8. Bode plots of discharging mode: (a) $\hat{i}_{S1}(s)/\hat{d}_{S1}(s)$, (b). $\hat{v}_o(s)/\hat{d}_{S2}(s)$.

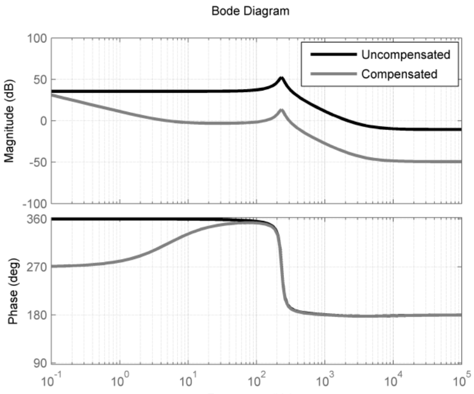


Fig. 9. Bode plot of charging mode: $\hat{v}_o(s)/\hat{d}_{Q0}(s)$

TABLE V
BODE PLOT PARAMETERS

V_o	48 V
$V_{bat} = V_{UC}$	36 V
$L_1 = L_2$	150μH
R_o	4.6 Ω
R_{dson}	3.8 mΩ
R_C	23 mΩ
D_{S0}	0.5
D_{S1}	0.67
D_{Q0}	0.25

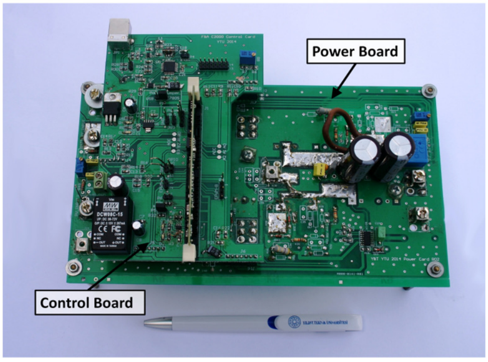


Fig. 10. 1kW prototype of the converter.

The proposed converter is tested for a battery/UC hybrid system as shown in Fig. 11. In this figure, the battery bank consists of three separate batteries in series thus it has 36V nominal voltage while UC has 48V rated voltage and 165F rated capacity.

A motor-generator set (for regenerative braking energy) and a dc load bank are connected to the output of the converter so as to attain the desired load profile. In this setup, a rectifier and an autotransformer are utilized to energize dc generator field winding. Furthermore, an oscilloscope and a power analyzer are used to retrieve experimental results.

Figs. 12-14 demonstrate the measured steady state waveforms for the discharging mode when the output power is set to 400 W. In this test, the battery current is controlled in a way that its power is 200W while UC is controlled to keep the dc bus voltage at 48V. It can be seen that these figures validate the theoretical analysis shown in Fig.3.

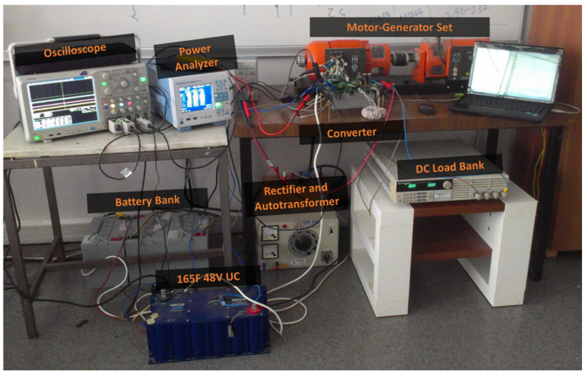


Fig. 11. Experimental setup

TABLE VI
PROTOTYPE POWER BOARD SPECIFICATIONS

d_{T0} range	0.4-0.6
Output voltage range	36-60 V
Input voltage range	22-40 V
Peak power	1 kW
Switching frequency	20 kHz
Output capacitor	2000μF, 100V and 23 mΩ ESR
Power Switches	FDP036N10A
Switch ratings	100 V/ 80 A
Power diodes	MBR4060PT
Diodes ratings	60 V/80 A
Gate drivers	FAN73933 and FAN73711
Gate voltages	15 V
Inductors	Kool-Mu Core, 150 μH, 40 mΩ ESR

Gate signals and related drain-source signals of each switch are given in Fig. 12. In Fig. 12, one can see that the duty cycle of T_0 is 0.5 according to the control strategy. Moreover, gate signals of S_1 (v_{GS-S1}) and S_2 (v_{GS-S2}) verify the analysis: v_{GS-S1} duty cycle (~0.73) becomes higher than v_{GS-S2} duty cycle (~0.66) due to the difference between battery and UC voltages.

Fig.13 illustrates L_1 and L_2 voltage and current variations. Inductor voltages and inductor currents vary according to states of switches. Moreover, both inductor currents are positive since both energy storage elements discharge.

The voltage and current of Q_0 body diode are illustrated in Fig.14. From Fig.14 and Fig.12, one can see that when T_0 is OFF, the diode starts to conduct as can be understood from its positive current. Conversely, when S_0 is ON, the diode becomes OFF thus its current goes to zero.

Figs. 15-16 illustrate the measured steady state waveforms when the converter operates in the charging mode. In this test, by controlling Q_0 switch, the output voltage is again kept at 48 V while UC is charged under 400W constant power. Based on these figures, it can be asserted that the experimental results match the theoretical waveforms given in Fig. 4.

Fig. 15 shows the experimental results of Q_0 terminal voltages at steady state. In Fig.15, the duty cycle of Q_0 is about 0.8 as expected according to (10) which explains the relationship between the duty cycle of Q_0, UC voltage (~40V), and the output voltage.

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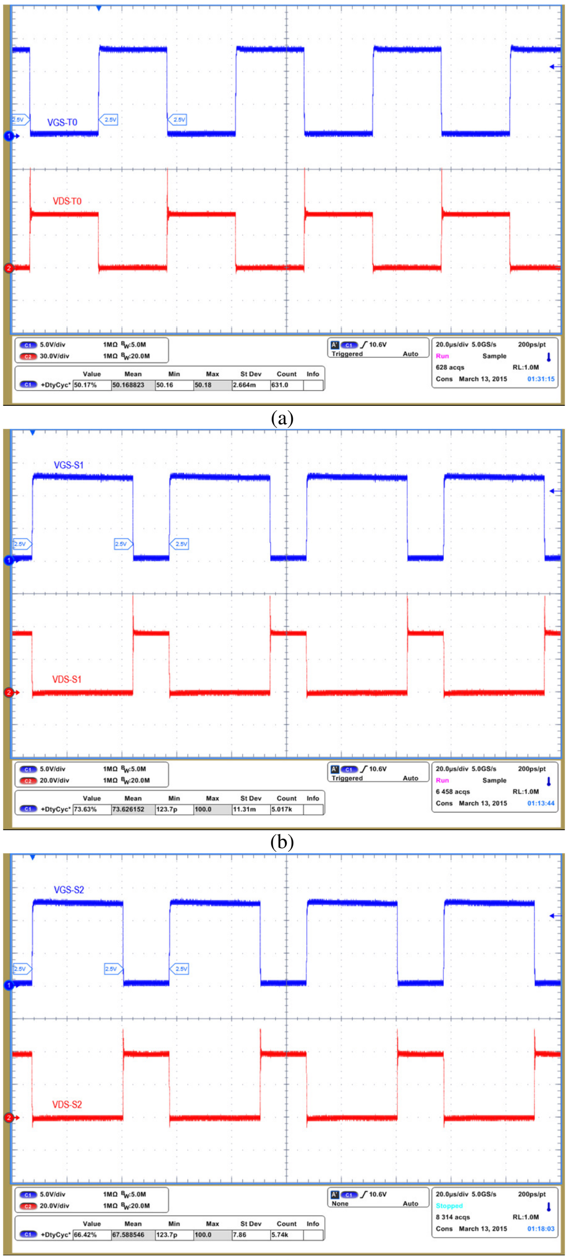
In Fig. 16, the voltage and current variations of L_2 are demonstrated. It can be noticed that the inductor current is negative since UC is charged. Moreover, when Q_0 is turned ON, the voltage of the inductor becomes negative thus its current increases (negatively); conversely, turning it OFF makes the voltage of the inductor equal to UC voltage and decreases its current (negatively).

Fig. 17 illustrates the proposed converter efficiency curves for the discharging and charging modes which are obtained by power analyzer. In the discharging mode, the power of one source is set to 200 W while other source is utilized to compensate the load demand. Besides, in the charging mode, dc bus is regulated when adjusting the charging power of the input source.

Fig. 17 clearly indicates that in both modes converter efficiency is higher than 93% under the whole power range. Furthermore, by comparing efficiency curves, one can see that the charging mode efficiency is higher than the discharging mode efficiency due to the difference between the number of controlled switches in these two modes.



(a)

(b)

(c)

Fig. 12. Experimental waveforms of switches gate-source and drain-source voltages in discharging mode: (a) S_0: $v_{GS\text{-}T0}$ [Ch1: 5V/div], $v_{DS\text{-}T0}$ [Ch2: 30V/div). (b) S_1: $v_{GS\text{-}S1}$ [Ch1: 5V/div], $v_{DS\text{-}S1}$ [Ch2: 20V/div]. (c) S_2: $v_{GS\text{-}S2}$ [Ch1: 5V/div], $v_{DS\text{-}S2}$ [Ch2: 20V/div]. Time base: 20μs/div.

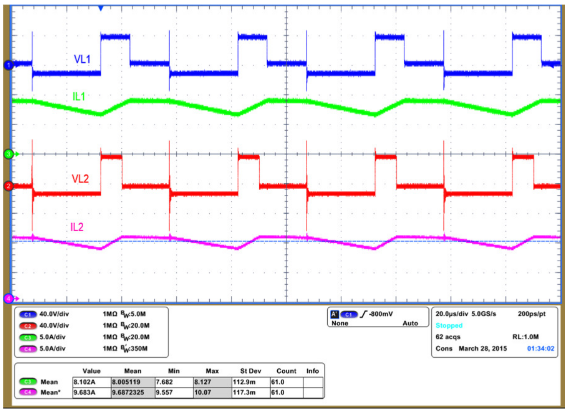


Fig. 13. Experimental waveforms of inductor voltages and currents in the discharging mode: L1: v_{L1} [Ch1: 40 V/div], i_{L1} [Ch3: 5 A/div], L2: v_{L2} [Ch2: 40 V/div], i_{L2} [Ch4: 5 A/div]. Time base: 20 μs/div

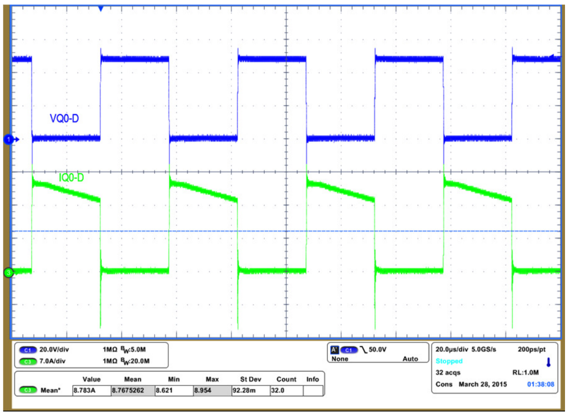


Fig. 14. Experimental waveforms of Q0 switch body diode voltage and current in the discharging mode: $v_{Q0\text{-}D}$ [Ch1: 20V/div], $i_{Q0\text{-}D}$ [Ch3:10A/div]. Time base: 20μs/div

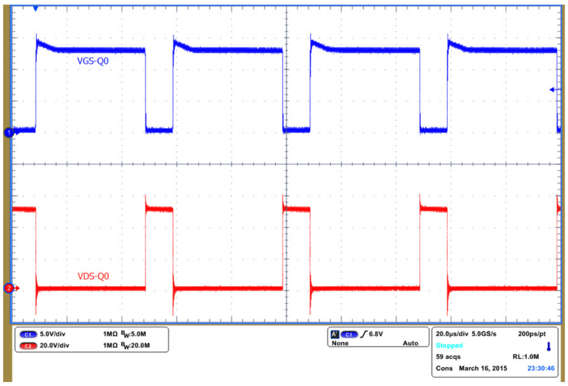


Fig. 15. Experimental waveforms of switch Q_0 gate-source and drain-source voltages in the discharging mode: (a) $v_{GS\text{-}Q0}$ [Ch1: 5V/div], $v_{DS\text{-}Q0}$ [Ch2: 20V/div). Time base: 20μs/div.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TVT.2015.2500683, IEEE Transactions on Vehicular Technology

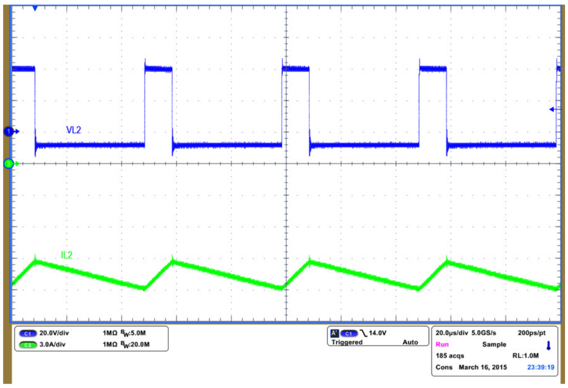


Fig.16. Experimental waveforms of inductor voltage and current in the charging mode: v_{L2} [Ch1: 20V/div], i_{L2} [Ch3: 3A/div]. Time base: 20μs/div.

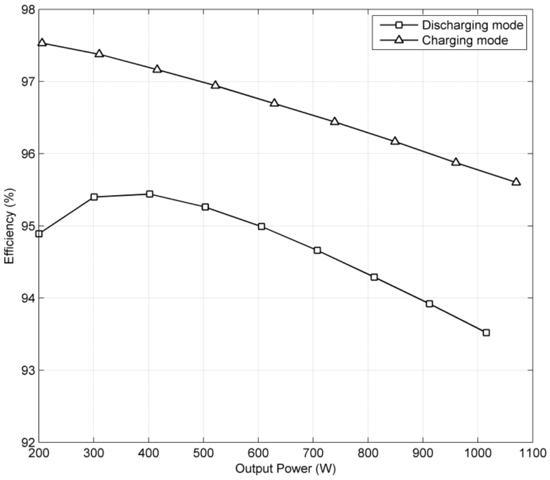


Fig.17. Efficiency curves

In order to test the dynamic performance of the system, a load profile is chosen according to normalized ECE-15 driving cycle [25]; the analyzed section of this driving cycle is demonstrated in Fig. 18. This period is chosen to examine the system under maximum power demand and in the presence of regenerative braking energy. The load profile is created by utilizing dc load bank and dc generator which are shown in Fig. 11.

Moreover, simulations are carried out via developed PSIM® switching model including switch turn-ON resistances and output capacitor equivalent serial resistance; in the simulation, battery and UC are modeled as in [25]. Note that in both cases battery and UC initial voltages are set to 38 V and 33.6 V (70% state-of-charge), respectively. Figs. 19-21 compare the experimental and simulation results.

In Fig. 19, the output voltage and output current are shown. Here, it is clear that the output voltage is successfully regulated at 48 V in both cases. Moreover, the fact that output current in the experiment and simulation match well indicates that the output power is adjusted as intended by load bank and generator

Fig. 20 shows the battery and UC average current. From Fig. 20, it can be noticed that the battery current variations in the experiment and in the simulation appear similar. In both cases maximum battery current is limited to 20 A due to the control strategy; at this instant, UC current is increased for compensating the load demand. Additionally, UC current becomes negative when it stores regenerative braking energy.

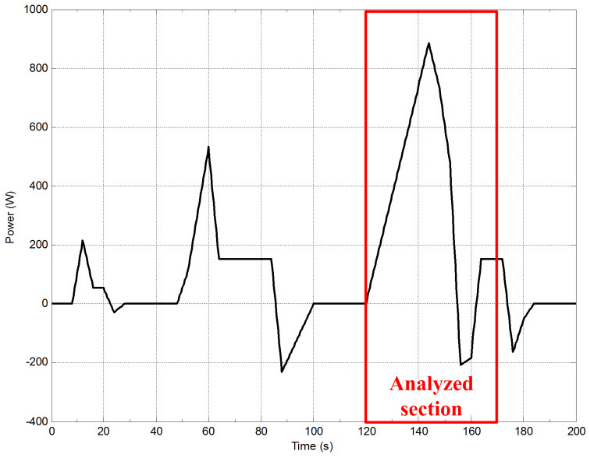


Fig.18. Normalized ECE-15 driving cycle and its analyzed section

Fig. 21 highlights the input source voltages. This figure indicates that battery voltage as well as UC voltage in the experiment and in the simulation change in a similar way. Because of its equivalent serial resistance, battery voltage decreases substantially when it gives power. In addition to that, UC voltage decreases when it compensates load demand and increases when it is charged.

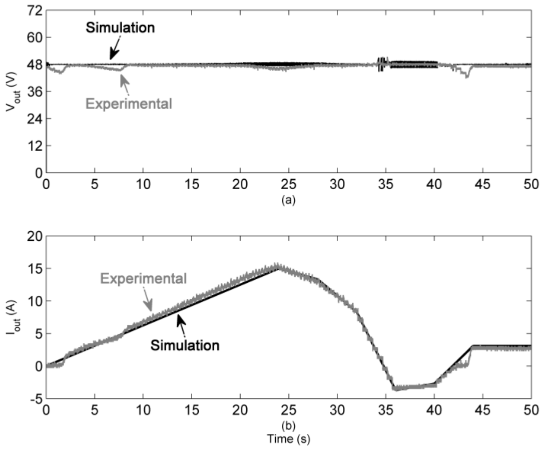


Fig.19. Dynamic test results: a) output voltage, b) output current.

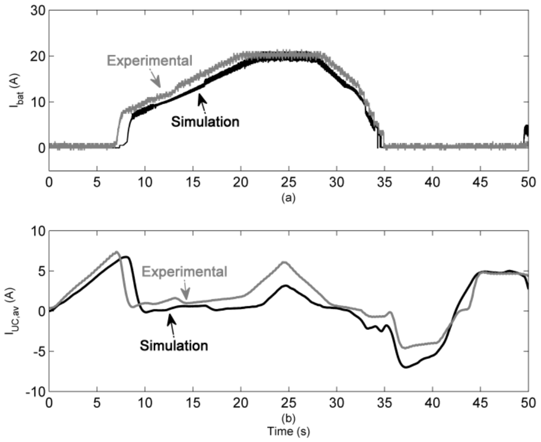


Fig.20. Dynamic test results: a) battery current, b) UC average current.

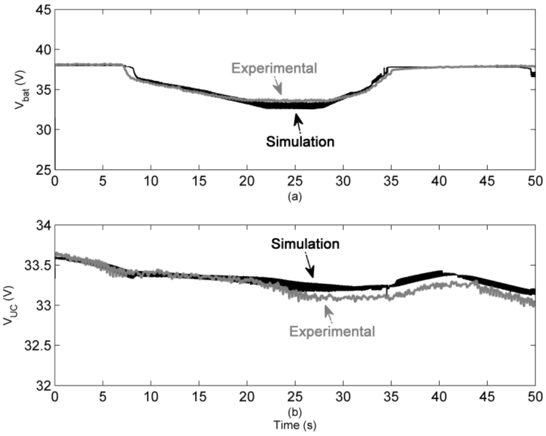


Fig.21. Dynamic test results: a) battery voltage, b) UC voltage.

VI. CONCLUSIONS

In this work, a new multi input non-isolated bidirectional dc/dc converter for hybrid energy storage systems to be used in electric vehicle applications has been proposed. A detailed comparison of the proposed converter and two conventional converters has been presented. The operation modes of the proposed converter have been analyzed thoroughly and small signal ac models for these modes have been obtained. For a battery/UC hybrid system, associated transfer functions have been derived for controlling battery current and regulating the output voltage. A 1 kW laboratory prototype of the proposed converter topology has been designed and developed. Utilizing derived transfer functions, PI controllers have been designed in order to achieve proper phase margins and cut-off frequencies. Experimental findings have revealed that the prototype converter efficiency is greater than 93% in both operation modes. The analysis has been validated through this prototype, and by comparing the experimental and simulations results, dynamic performance of the converter has been examined under a load profile obtained from a well known driving cycle, namely ECE-15. For a future work, it is aimed to build a full scale battery/UC hybrid system based on the proposed converter and test it in a concept electric vehicle.

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Furkan Akar (S'10) was born in Kocaeli, Turkey, in 1986. He received the B.Sc. degree in electrical and electronics engineering from Mersin University, Mersin, Turkey, in 2009, the M.Sc. degree in electrical engineering from Florida State University, Tallahassee, FL, USA, in 2012. He is currently a Ph.D. candidate at Department of Electrical Engineering, Yildiz Technical University, Istanbul, Turkey. His field of research includes control of the switched reluctance machine, renewable energy sources, dc-dc converters, electric vehicles, and hybrid energy storage systems.

Yakup Tavlasoglu was born in Erzurum, Turkey, in 1987. He received the B.Sc. degree in electronics engineering from Gebze Institute of Technology, Kocaeli, Turkey, in 2011. He is currently a M.Sc. student at Department of Electrical Engineering, Yildiz Technical University, Istanbul, Turkey. His research interests are photovoltaic systems, dc-dc converters, electric vehicles, and hybrid systems.

Enes UGUR (S'11) received the B.Sc. degree in electrical engineering from Istanbul Technical University in 2008 and the M.Sc. degree from Yildiz Technical University, Istanbul, Turkey, in 2011. He is currently a Ph.D. student at Department of Electrical Engineering, Yildiz Technical University. His research interests include fuel-cells, electric vehicles, dc-dc converters, energy management strategies for renewable energy systems, and fault diagnosis of wide-bandgap devices.

Bulent VURAL received the B.Sc., M.Sc. and Ph.D. degrees from Yildiz Technical University, Istanbul, Turkey, in 2004, 2007, and 2010, respectively, all in electrical engineering. He is an Associate Professor and director of Electric Vehicle Technologies Laboratory at Yildiz Technical University. His research interests are; embedded control systems, power electronics applications in alternative/renewable energy systems and electric vehicles, smart grid, power hardware-in-the-loop simulations. He is author and coauthor of more than 35 journal and conference papers.

Ismail AKSOY was born in Cologne, Germany, in 1977. He received the B.Sc., M.Sc., and Ph.D. degrees in electrical engineering from Yildiz Technical University, Yildiz, Turkey, in 1999, 2001, and 2007, respectively. He was a Research Assistant from 1999 to 2008 in the Department of Electrical Engineering, Yildiz Technical University. Since 2014 he has been working as an Associate Professor in the Department of Electrical Engineering at Yildiz Technical University. He has published over 20 journal and conference papers in the area of power electronics. He was also employed in three research projects concerning power electronics. His research subjects are power factor correction, switching power supplies, high frequency power conversion, and active and passive snubber cells in power electronics.